EUV – Supporting Moore's Law

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Forward looking statements

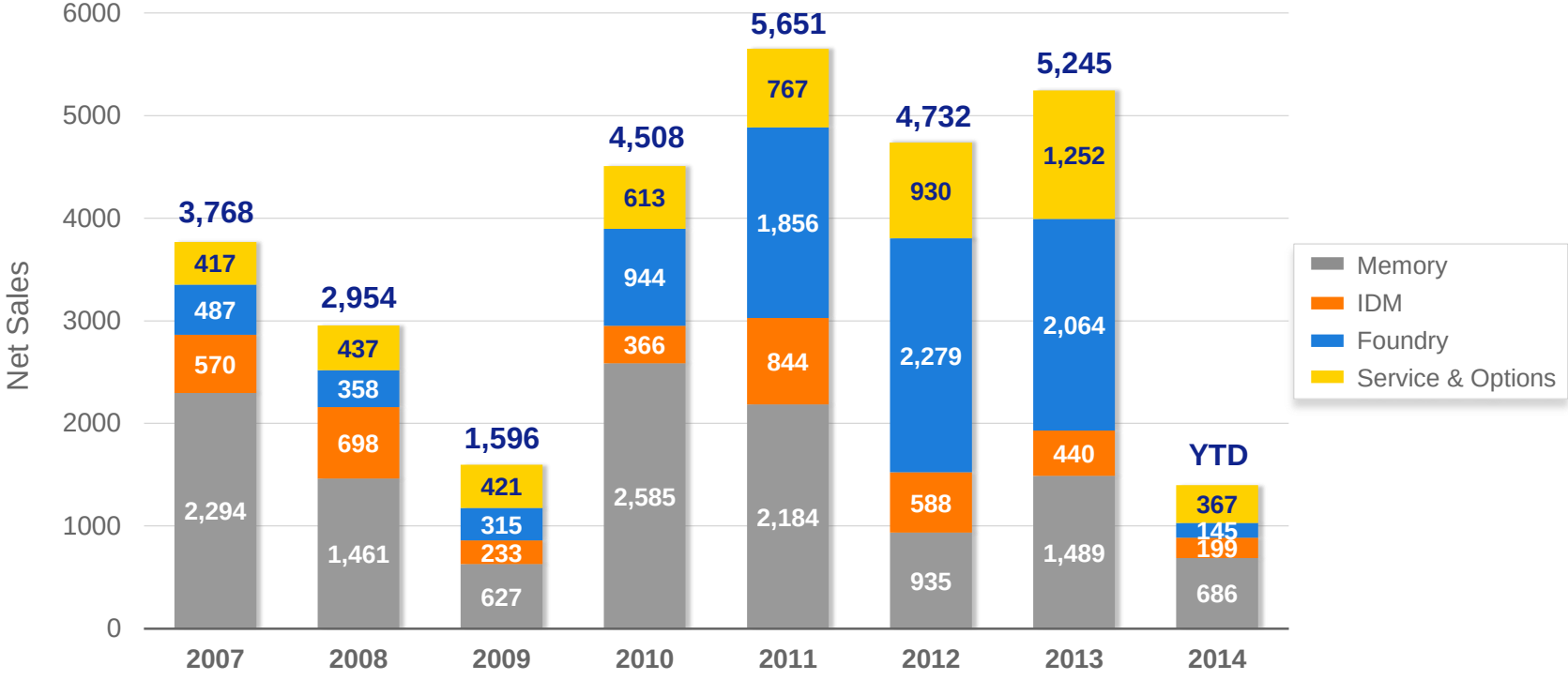
“Safe Harbor” Statement under the US Private Securities Litigation Reform Act of 1995: the matters discussed in this document may include forward-looking statements, including statements made about our outlook, expected sales levels, IC unit demand, forecasted industry developments, including expected bit growth in 2014, expected semiconductor sales and expected smartphone, tablet and PC use in future years, expectations on development of the shrink roadmap across all of our systems, expected number of EUV systems to be recognized in 2014, expectations on timing for volume production for EUV systems and other statements about the expected development of EUV technology and its adoption by our customers.

These forward looking statements are subject to risks and uncertainties including: economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors (the principal product of our customer base), including the impact of general economic conditions on consumer confidence and demand for our customers' products, competitive products and pricing, the impact of manufacturing efficiencies and capacity constraints, the continuing success of technology advances and the related pace of new product development and customer acceptance of new products, our ability to enforce patents and protect intellectual property rights, the risk of intellectual property litigation, availability of raw materials and critical manufacturing equipment, trade environment, changes in exchange rates, available cash, our ability to successfully integrate Cymer, and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission.

Content

- Semiconductor environment
- Challenges of shrink
- Our response: the lithography roadmap

ASML total net sales M€ by End-use



Numbers have been rounded for readers' convenience

Business environment for 2014

NAND

- Bit growth forecast mid 40s% driven by SSD drives and smartphones
- Demand being met through shrink and capacity expansion
- Challenges in qualification of vertical NAND and future node planar technologies, creating litho demand timing uncertainty

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DRAM

- Bit growth forecast of 20 - 30%
- Bits supplied by planned technology transitions meet bit demand forecast
- Litho process intensity increases due to node transition and mobile DRAM process complexity

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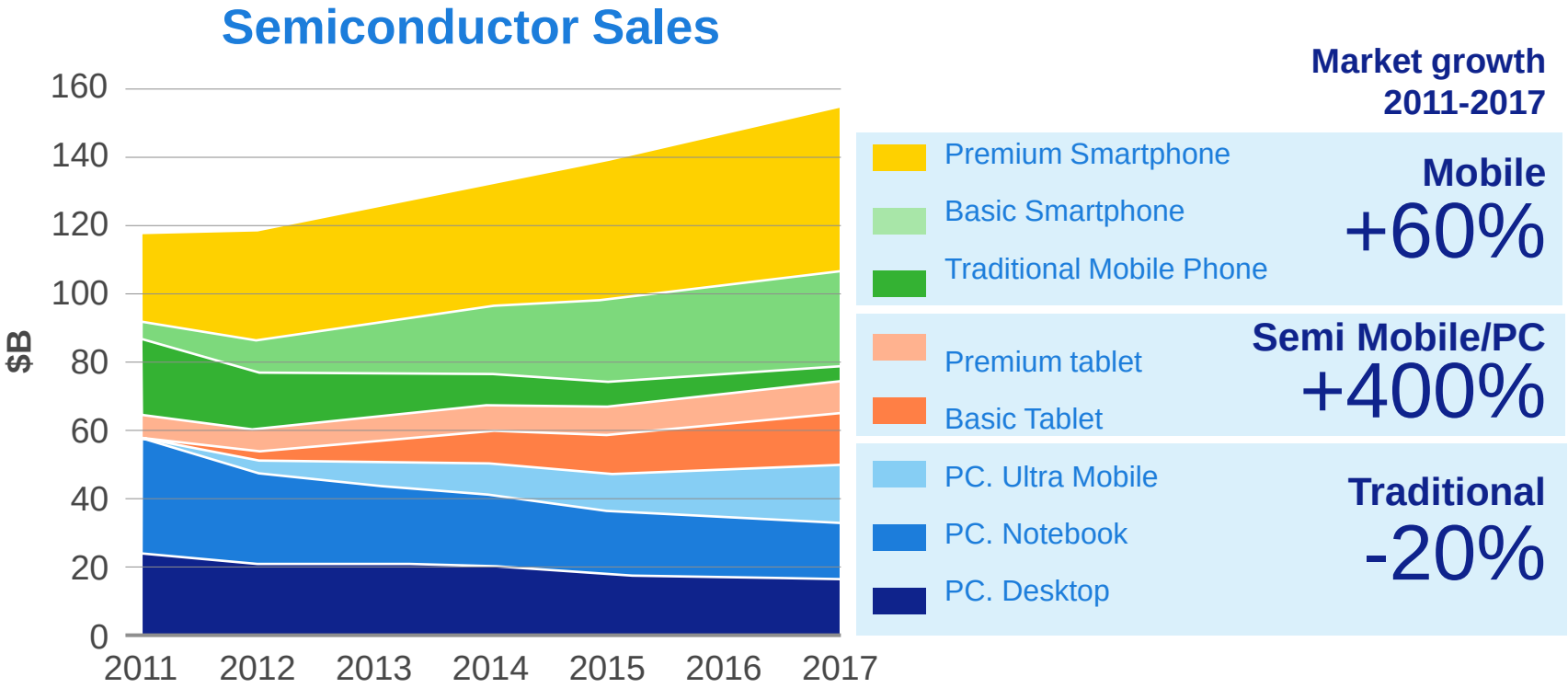
LOGIC

- Customers are installing capacity for their 20/16/14 nm nodes
- Timing uncertainty in next generation device designs and production ramps

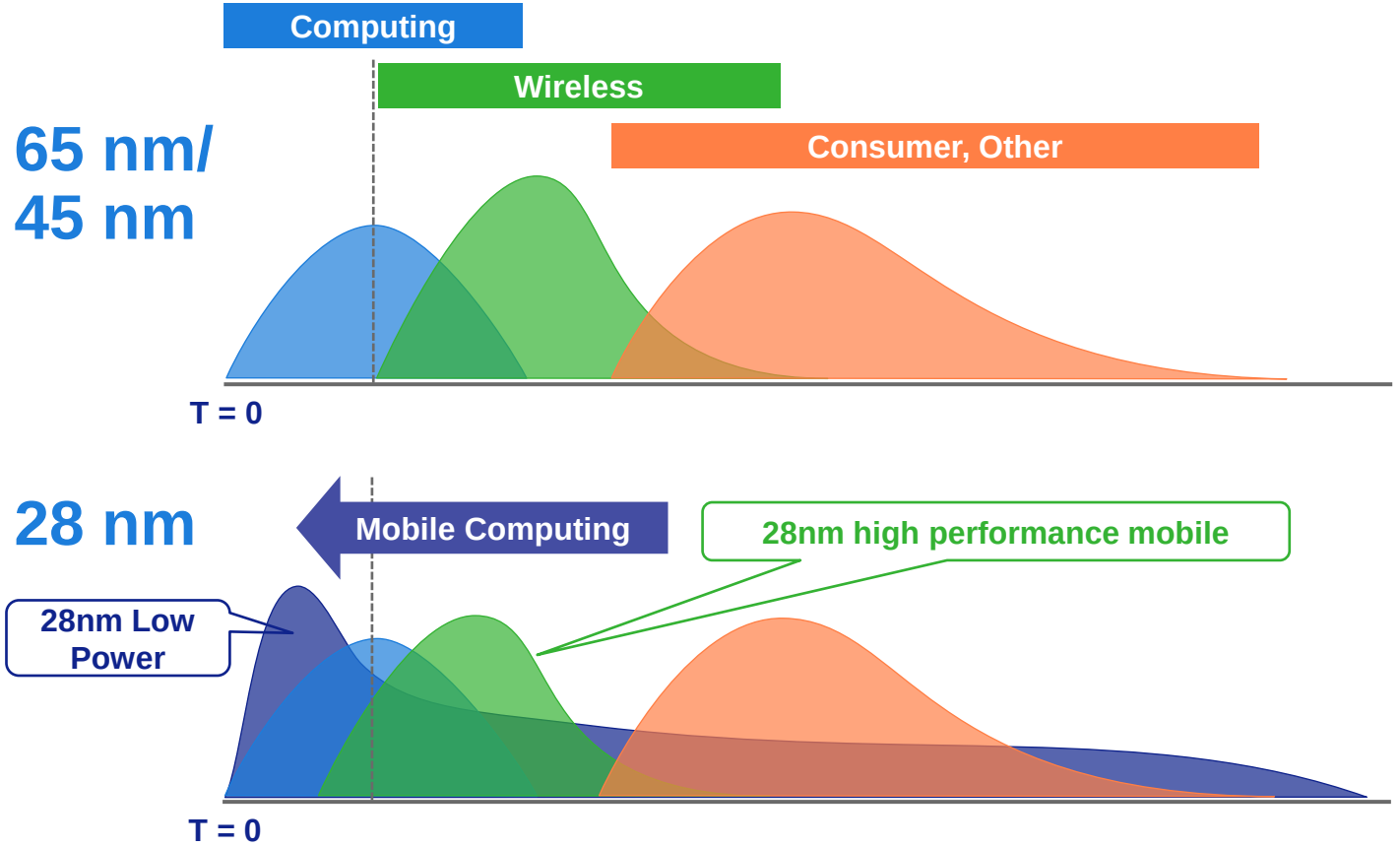
Longer term Logic growth is in Mobile

Creating Logic market share battles



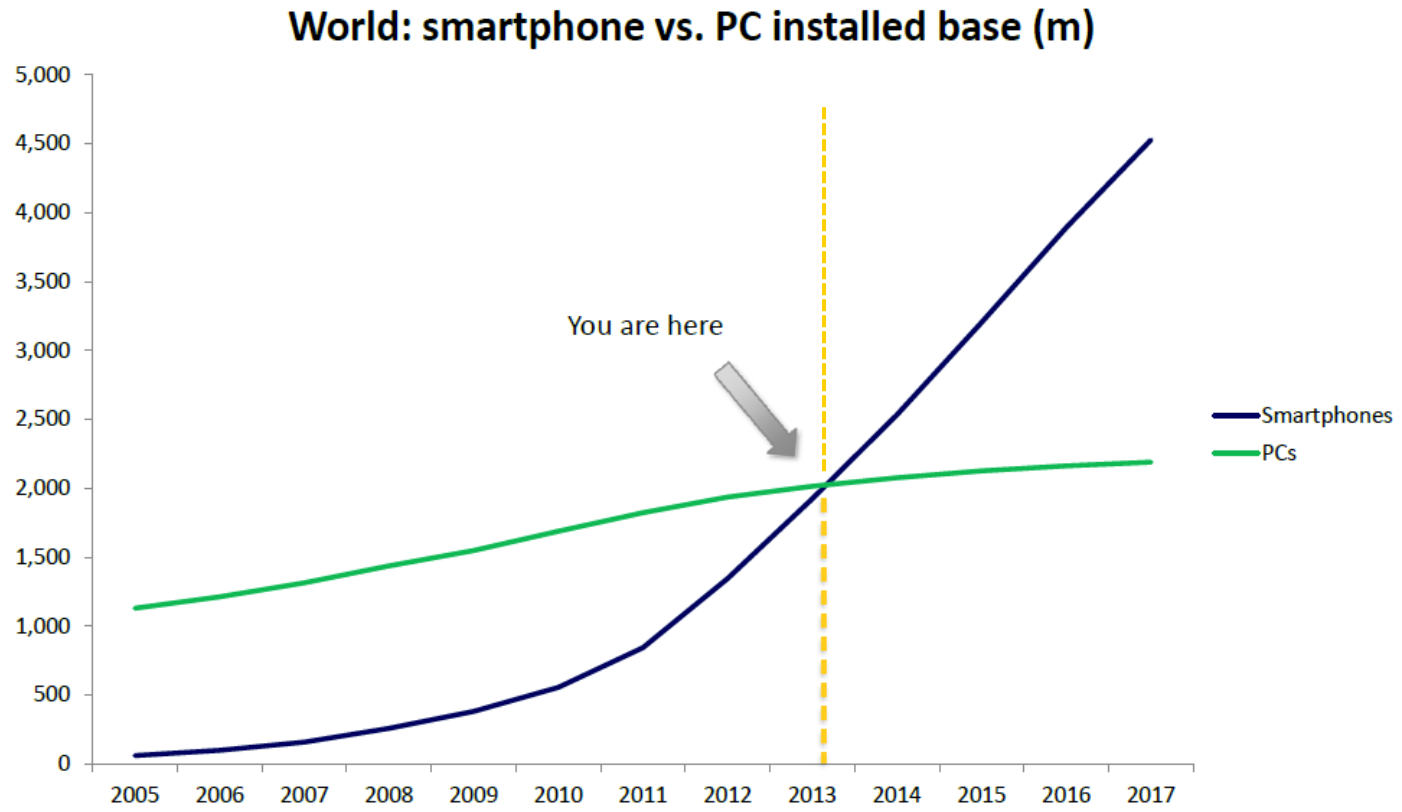
Source: Bob Johnson,Gartner, ISS, Jan 2014

Low power starts to drive the technology roadmap



Source: Geoffrey Yeap, Qualcomm, IEDM, Dec 2013

The Smartphone boom
Foundries and fabless drive the logic market



Source: IHS Electronics & Media, January 2014

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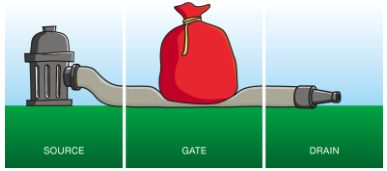
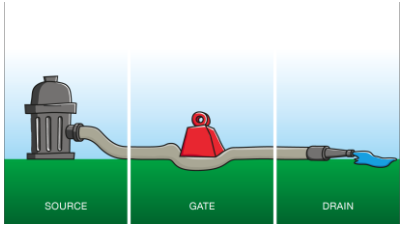


No end in sight for logic scaling

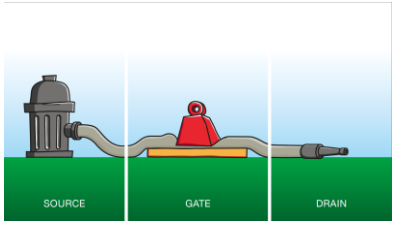
N20

Bulk CMOS:
Complementary Metal Oxide Semiconductor



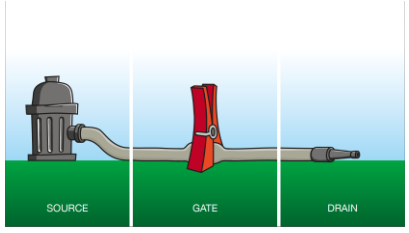
N20 / N14

SOI:
Silicon on Insulator



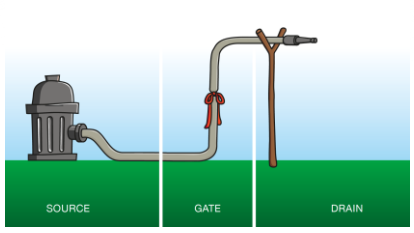
N1x / N7

Bulk FinFet :
Fin field effect transistor



N7 / N5

SOI FinFet :
Silicon on insulator fin field effect transistor, III-V

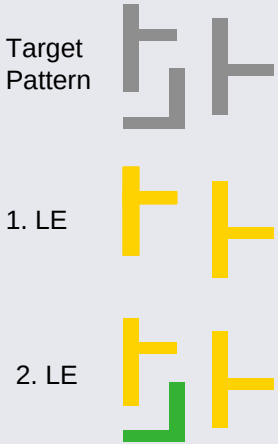
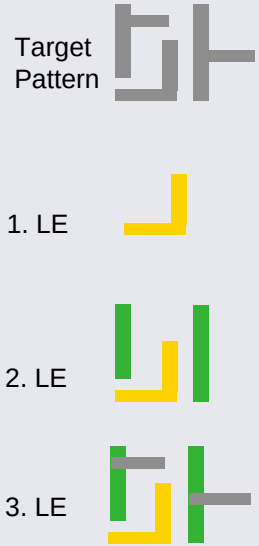
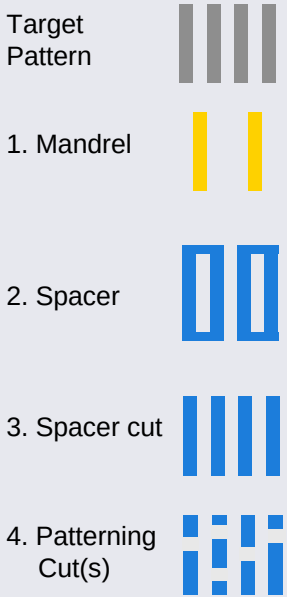
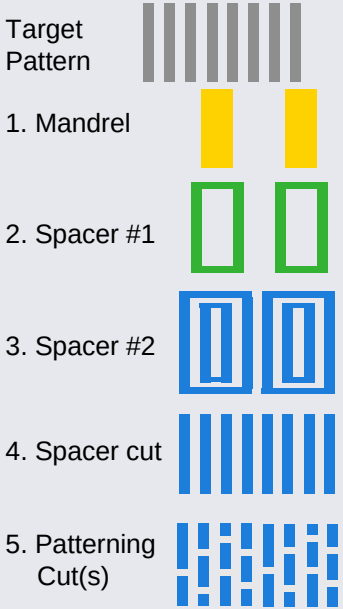


N5 / N3.5

Gate-all-around transistor

Current scaling requires “Sub-resolution” imaging

Sub-resolution imaging requires multiple litho steps

	2D Litho-Etch (LE^N) Multi Patterning		1D Self Aligned Multiple Patterning (SAMP)	
	LE^2 (LELE)	LE^3 (LELELE)	SADP (D=Double)	SAQP (Q=Quadruple)
Process Flow				
	• Suitable for 1D or 2D patterning • Overlay control of each layer is a key		• Suitable for 1D layout. (← better CD, LWR control) • May need multiple cut patterns	

Content

- Semiconductor environment
- Challenges of shrink
- Our response: the litho roadmap

Our Challenge: enable affordable scaling

- Scaling needs to create **lower cost and improved performance – ie., support Moore's Law**
- Affordable scaling in lithography can be achieved:
  - In the near term **- Immersion**: drive **productivity and yield (overlay and focus control)** with multiple patterning using advanced litho equipment extended with application products - Holistic Lithography/Yieldstar
  - In the mid/long term **- EUV:** drive **productivity/availability** and improve **operational cost**

Affordable shrink roadmap

2012 2013 2014 2015 2016 2017 2018 2019 2020

Immersion

EUV

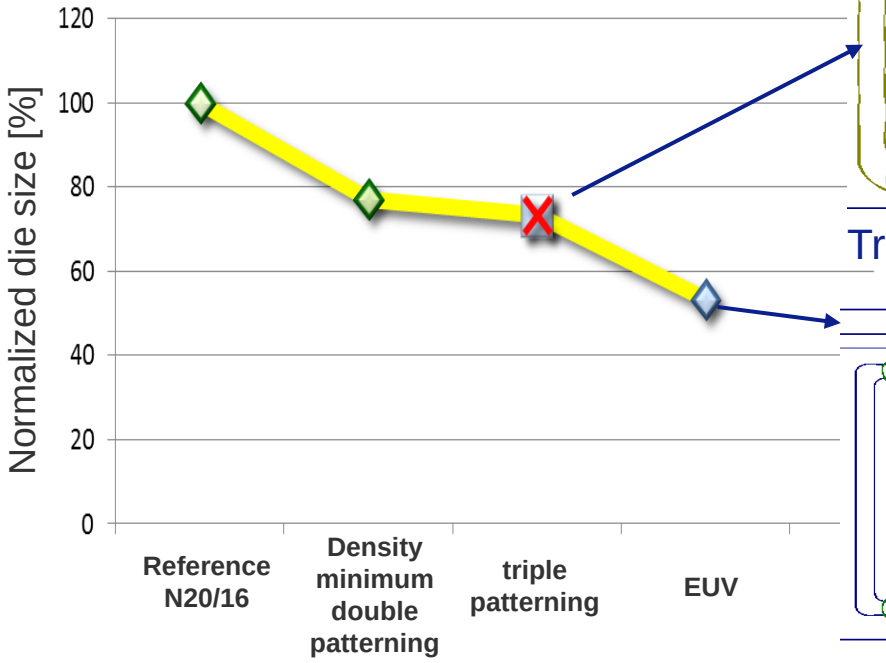
ArF Dry
KrF

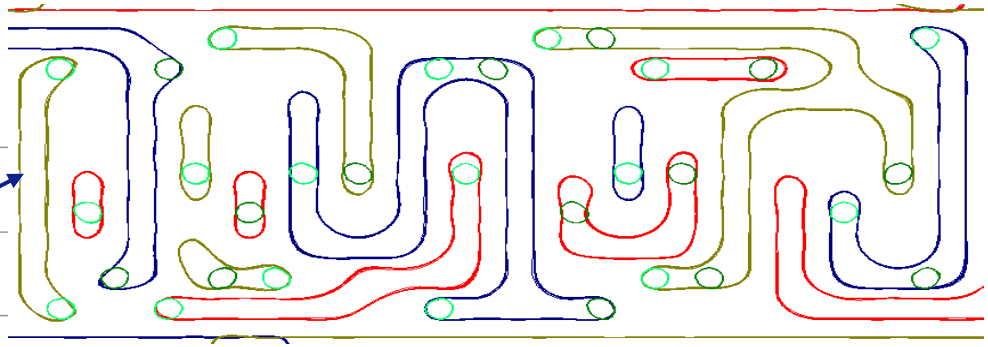
Supported by a Holistic Lithography approach using computational litho, overlay and CD metrology, feedback loops for wider process window creation and process control

Overlay … 1460K system
… system)
Extend the productivity … critical KrF (XT:860L/800-3D): memory applications

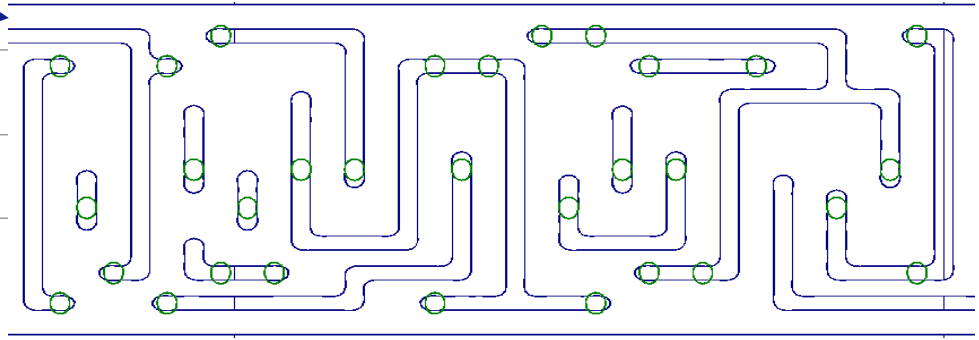
One year ago we thought…….
50% scaling for 10 nm logic node only with EUV

Shrink limited to ~25% using immersion due to layout restrictions and litho performance





Triple patterning does not show process window



EUV meets all litho requirements

Source: ARM, Scaled N20 nm flip-flop design

One year ago we thought…….
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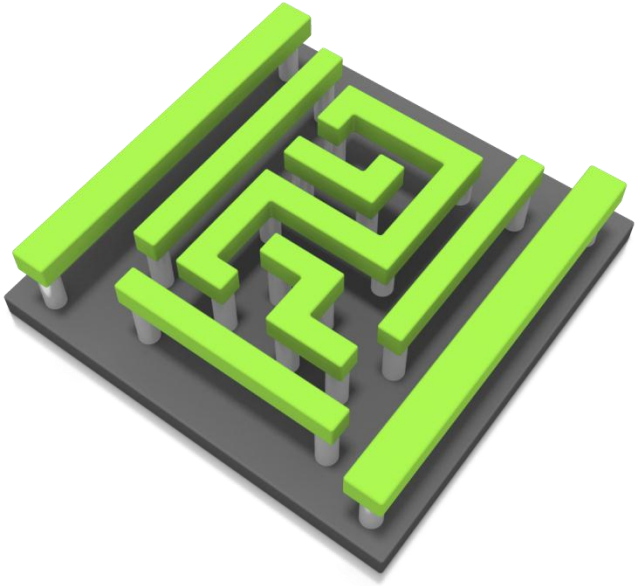
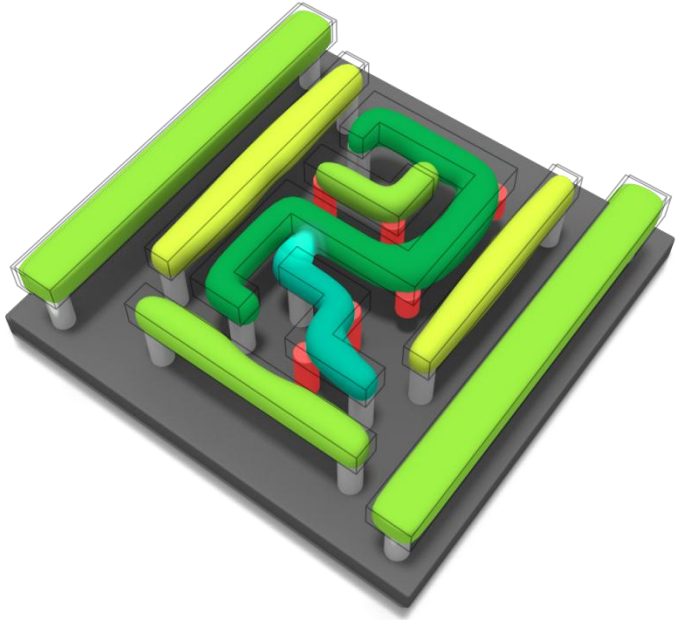
Shrink limited to ~25% using immersion due to layout restrictions and litho performance



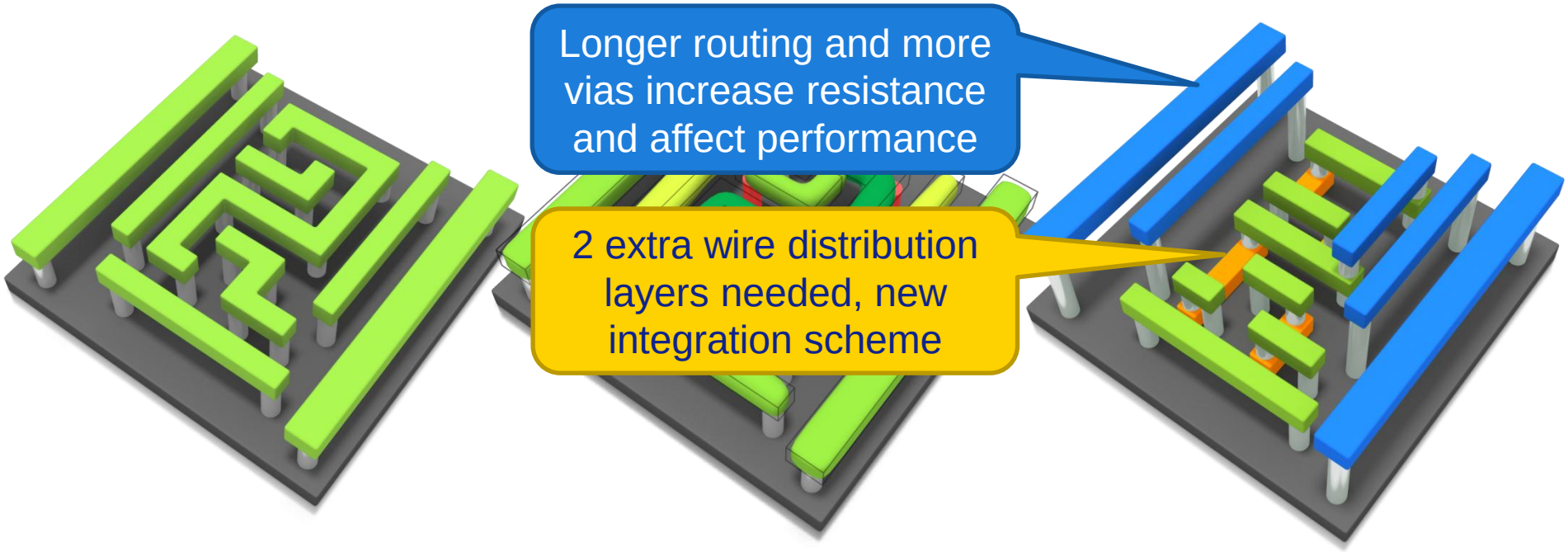
EUV 2D metal structure
Single layer solution



ArFi 2D metal structure
3-4 exposures, single layer
insufficient patterning fidelity

Today immersion extensions at 10 nm node possible with 1D

But critical metal layers require extra wiring layers, adding processing complexity and cost; decreasing chip performance



EUV 2D metal structure
Single layer solution

ArFi 2D metal structure
3-4 exposures, single layer
insufficient patterning fidelity

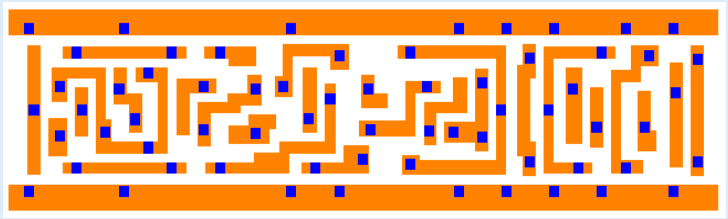
ArFi 1D metal structure
6-9 exposures in 3 layers

10nm logic design can be done in 1D design w/ immersion

But at the cost of 15% larger dies at comparable design rules

2D

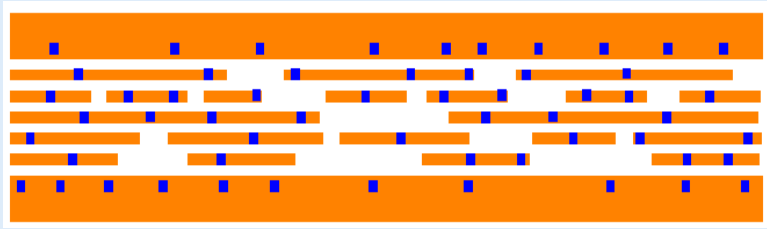
Die Size: 100%



EUV

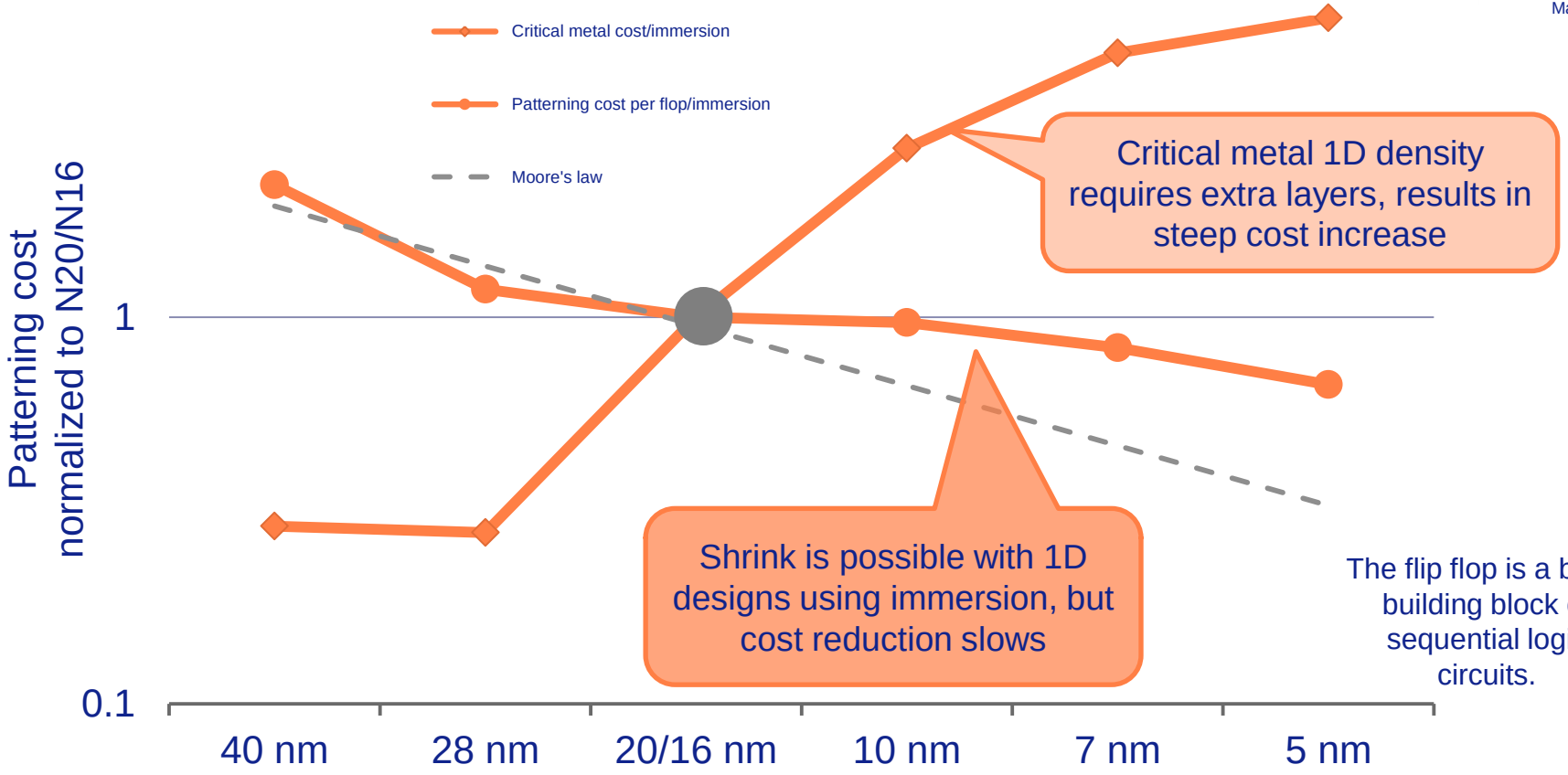
1D

Die Size: 115%



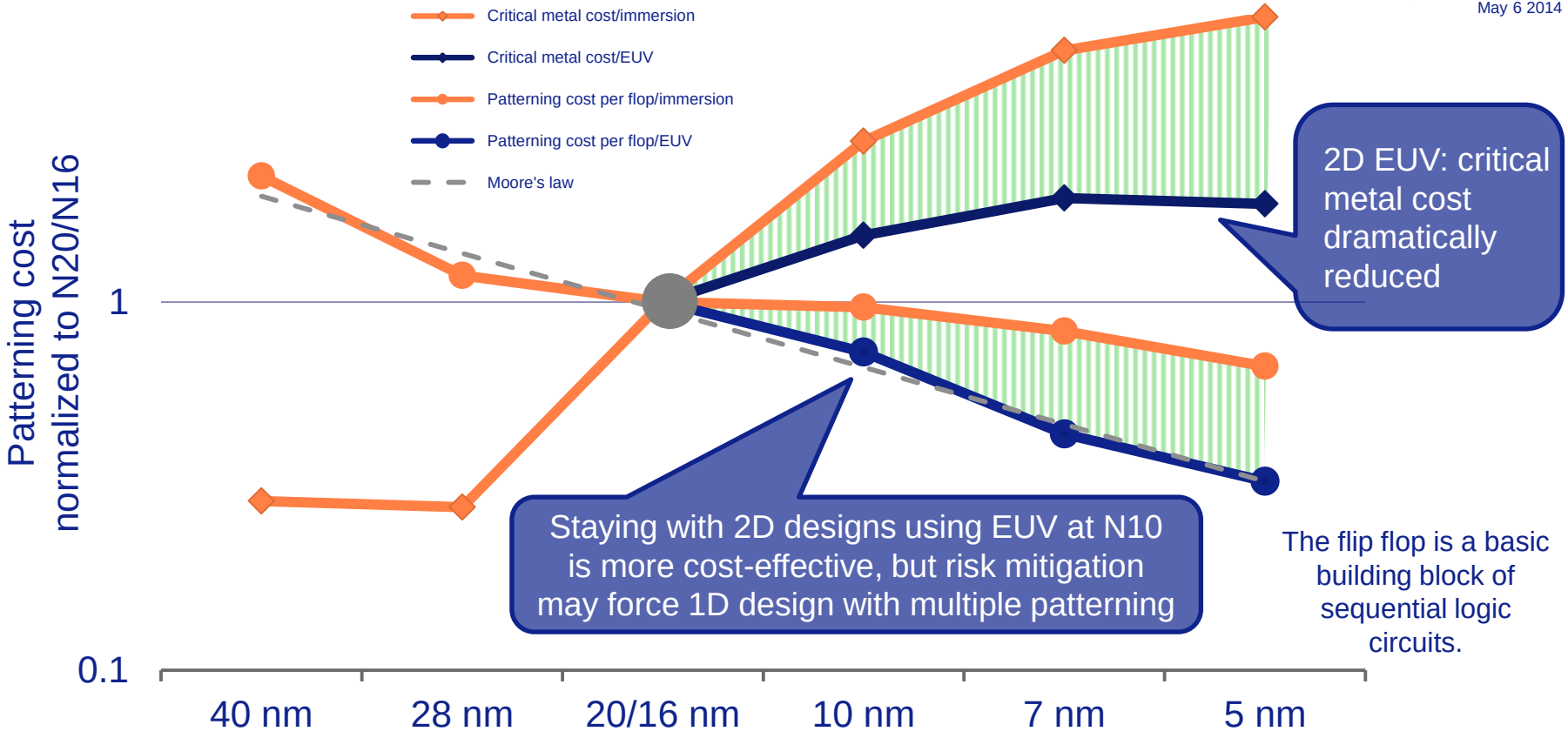
Immersion multi-pass patterning

Cost: 1D/immersion vs 2D/EUV



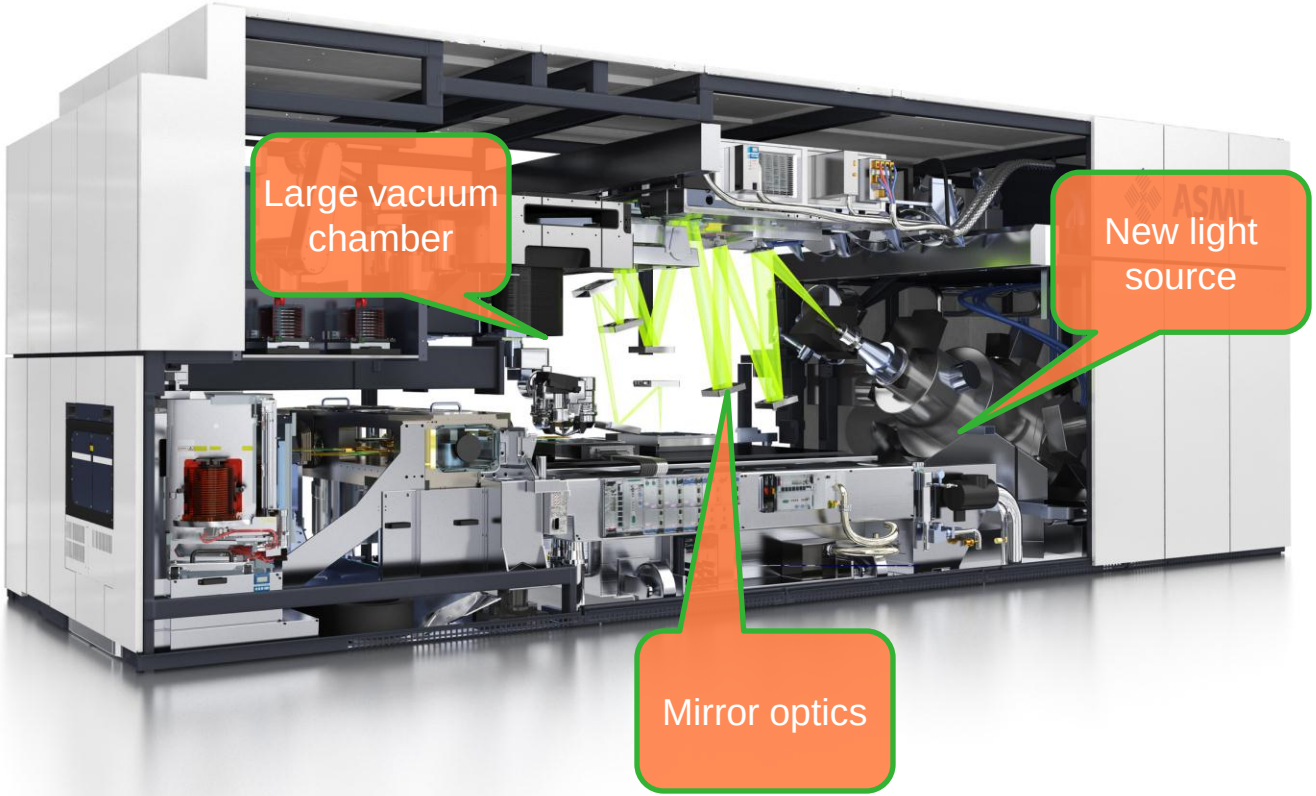
The flip flop is a basic building block of sequential logic circuits.

Cost: 1D/immersion vs 2D/EUV



The flip flop is a basic building block of sequential logic circuits.

EUV: Evaluations for 10nm process insertion underway

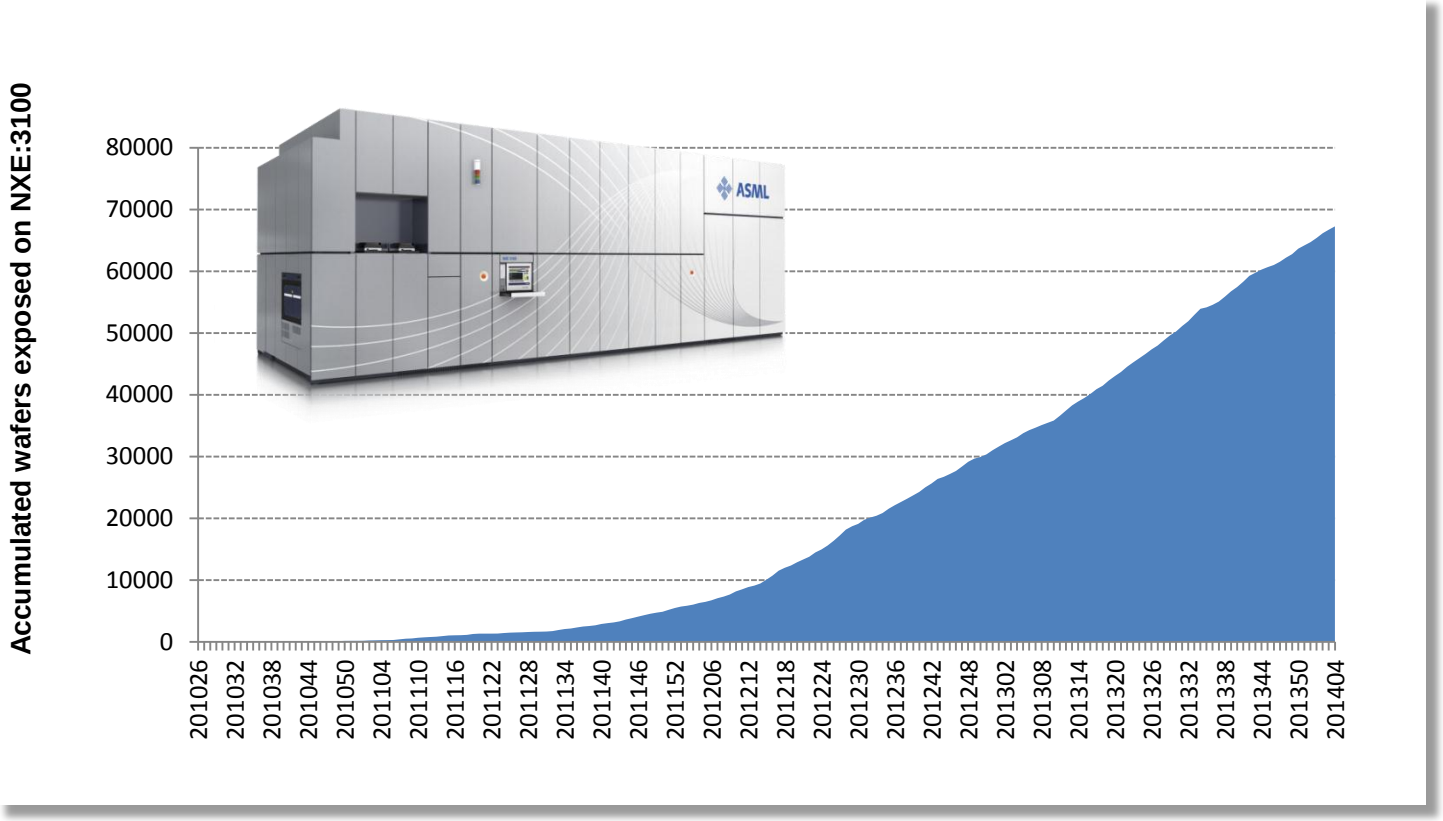


EUV – progress toward production insertion

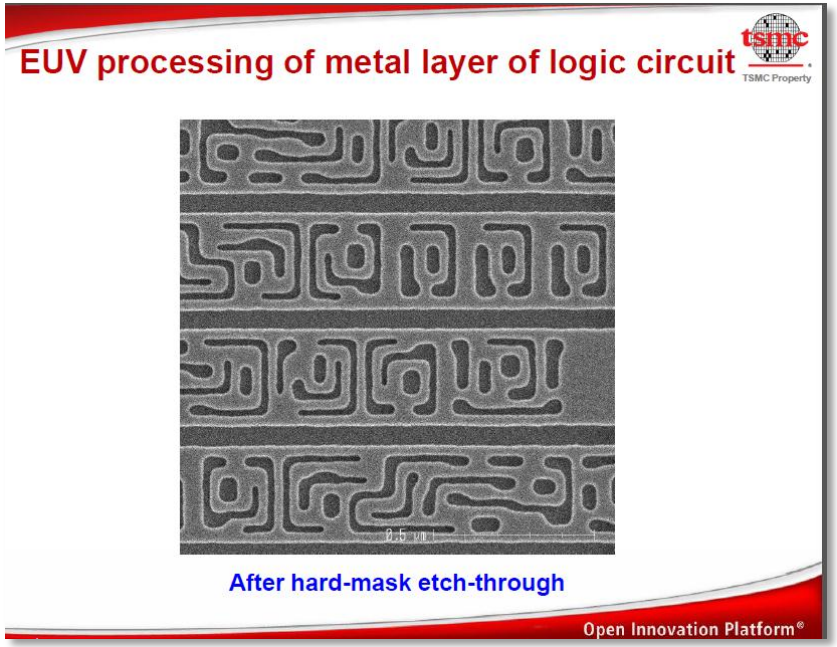
- Customers are qualifying EUV for insertion at the 10 nm logic node
- For process development, customers typically require 100 wafers per day, increasing to 500 wafers per day on average for production qualification
- We have provided customers with process development capability
- In 2016 we will provide our customers with the productivity needed for volume production, 1500wpd -> 2000wpd
- Our target is to recognize a total of 8 EUV systems in revenue this year

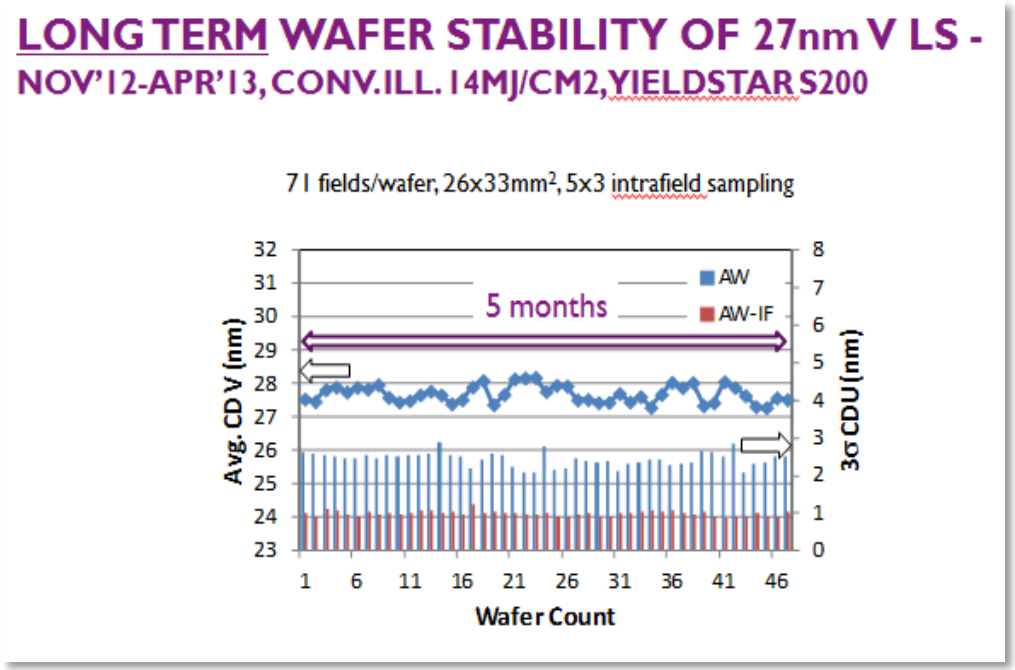
NXE:3100 in use for cycles of learning at customers

6 systems operational at customers for multiple years



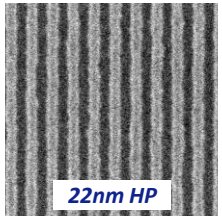
NXE:3100 shows stable performance and is used for device development at customer sites



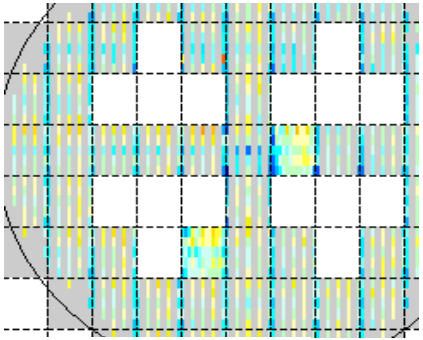


Data courtesy of TSMC and imec – EUVL Toyama 2013

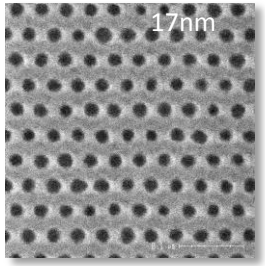
NXE:3300B Excellent single exposure imaging performance

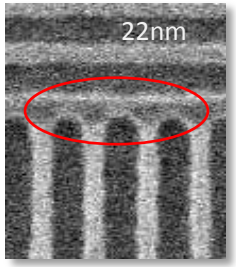


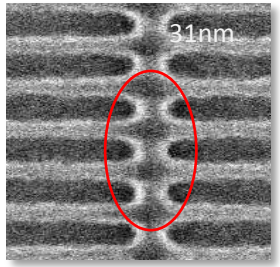
BE = 15.9 mJ/cm²
EL = 13%
DoF = 160 nm



Full wafer CDU = 1.5nm

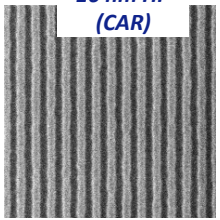


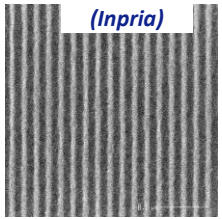


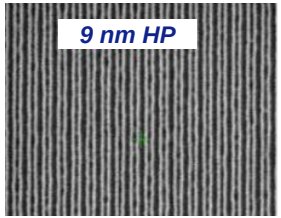


2D Contact

Tip-Line, Tip-Tip

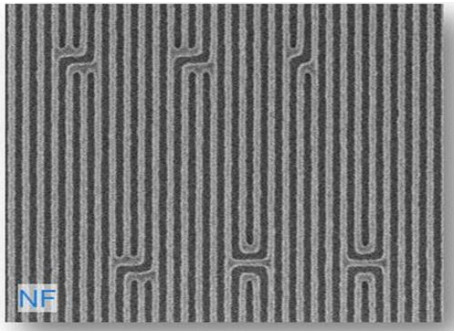






1D line spaces

EUV Spacer



10nm Metal 1

Node definitions:
Foundry Logic Node: “14nm” moved to “10nm”

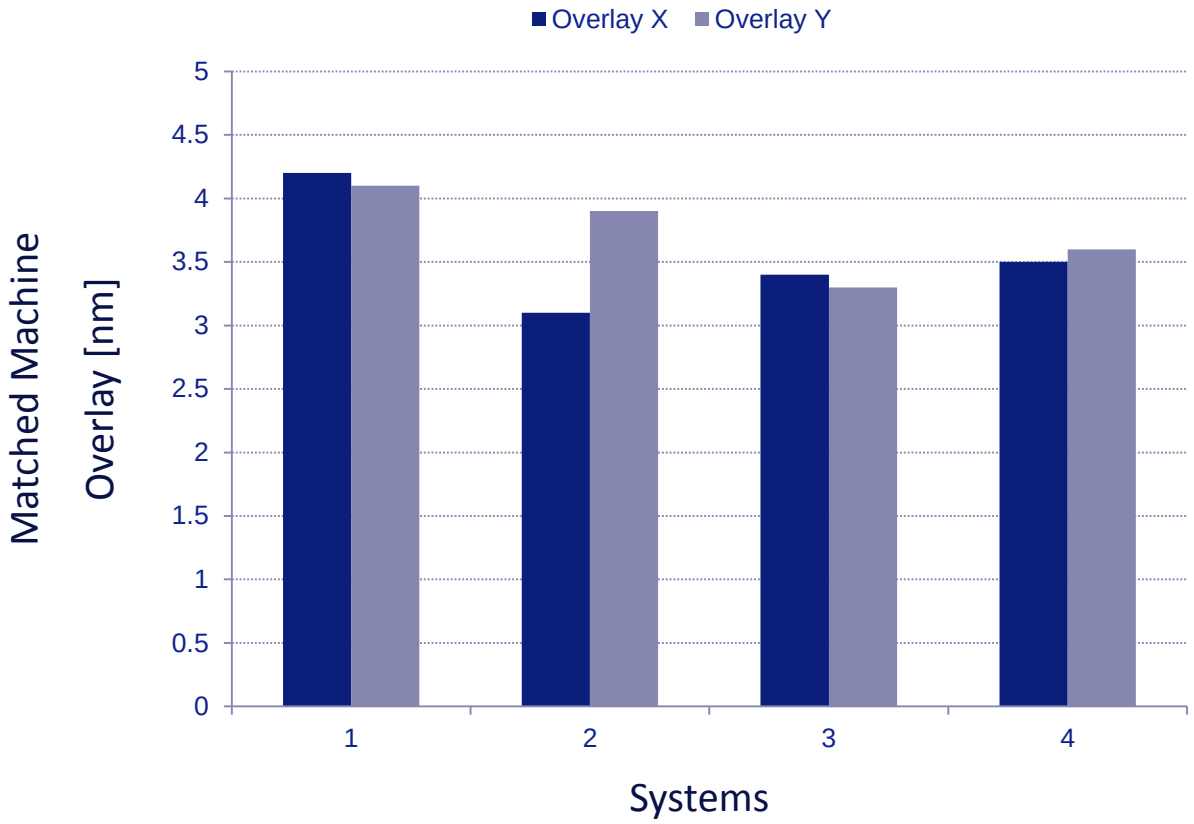
- Foundry Logic has inserted FinFET at 20nm node as a performance enhancement & now label this node “14nm or 16nm”
- Therefore, 10nm node is now the old 14nm requirements

Orig Node	28nm	20nm	14nm	10nm	7nm	5nm
M2 half pitch (nm)	53	32	23	16-20	11-15	8-14

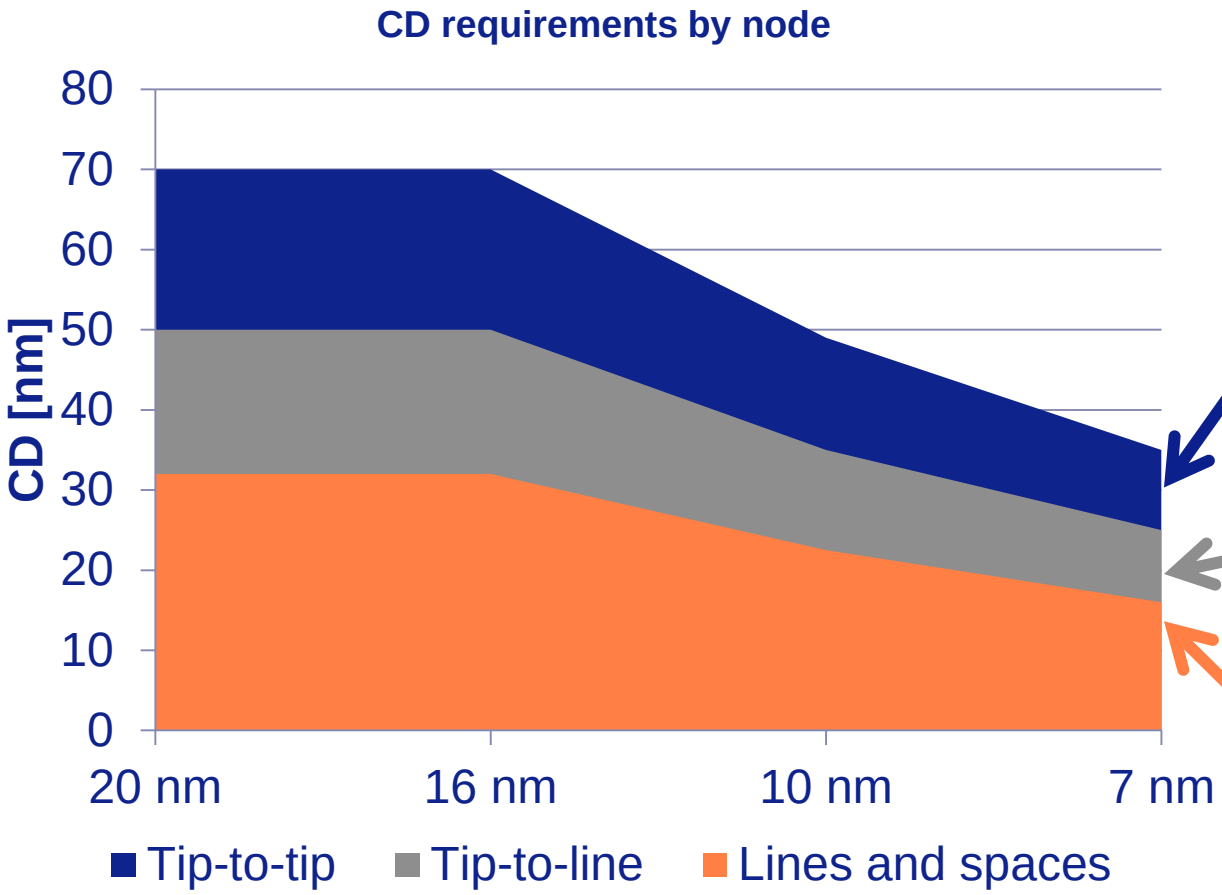
20nm FinFET

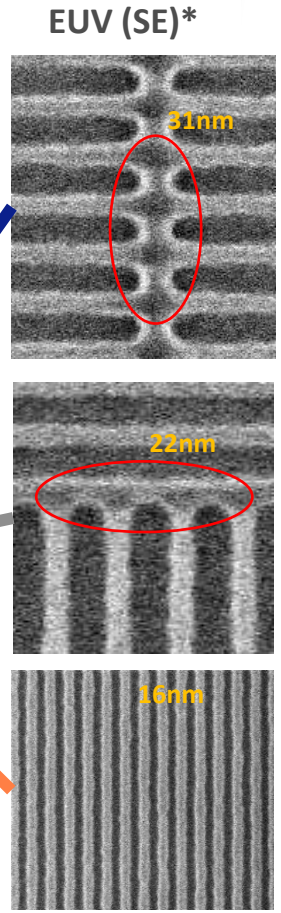
New Node	28nm	20nm	16/14nm	10nm	7nm	5nm
M2 half pitch (nm)	53	32	32	23	16-20	11-15

NXE:3300B showing excellent matched machine overlay performance on multiple systems to immersion



EUV meets aggressive 2D logic imaging requirements





** using high dose resist @ ~50mJ*

EUV (NXE:33x0B) system status overview

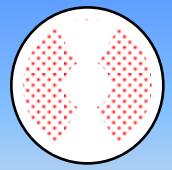
- **Multiple NXE:3300B systems fully qualified**
  - **2 systems exposing wafers at the customer sites**
  - **3 systems under install**

- **6 more NXE:3300B systems being integrated**
- **First NXE:3350B system has been started**

- **EUV cleanroom extension is under construction**

NXE technology roadmap - extendibility to <7nm (half pitch)

Half pitch						Under study			
Resolution [nm]		32	27	22	16	13	10	7	<7
Wavelength [nm]		13.5							
Lens	NA	0.25		0.33			0.33NA DPT		
								>0.5NA	
	flare	8%		6%	4%				
Illumination	coherence	σ=0.5	σ=0.8	σ=0.2-0.9	Flex-OAI	Extended Flex-OAI			
						reduced pupil fill ratio			
Overlay	DCO [nm]	7	4.0	3.0	1.5	1.2	1.0		
	MMO [nm]	-	7.0	5.0	2.5	2.0	1.7		
TPT (300mm)	Dose [mJ/cm^2]	5	10	15	20	20	20		
	Power [W]	3	10 - 105	80 - 250	250	250	500		
	Throughphut [w/hr]	-	6 - 60	50 - 125	125	125	165		



pupil fill ratio defined as the bright fraction of the pupil

EUV results summary and status

Summary

- **NXE:3300B** operational and exposing wafers at customer sites
- Performance fit for customer development 10nm Logic (and sub-20nm DRAM) and beyond

Status

1. EUV lithography technology is proven and is entering the industrialization phase
2. The EUV qualification requires 100 wafer per day output, which is determined by:
   a) Power: Supporting 30 wafers per hour
   b) Availability: Of greater than 50%
3. For pre-production customers have asked us to deliver 500 wafers per day by the end of 2014.
4. The full market potential of EUV will be realized at 125 wafers per hour and system availability > 90%. This will happen as a result of series of stepped through-put and reliability/availability upgrades.
5. The value of EUV is undisputed as the lithographic shrink technology of choice for multiple-nodes starting in 2016/2017.
6. Our customers and peers continue to support and drive development of EUV systems and infrastructure for introduction of EUV into volume production in the stated timeframe.